25.7 An IP2 Improvement Technique for Zero-IF Down-Converters

Hooman Darabi, Hea Joung Kim, Janice Chiu, Brima Ibrahim, Louie Serrano

Broadcom, Irvine, CA

Second order distortion remains an important issue in direct-conversion receivers. In cellular standards such as GSM, it imposes a very stringent IIP2 requirement on the receiver, and consequently on the down-converter [1]. On the other hand, optimizing the mixer to meet the required IIP2 [2] often compromises its other parameters such as headroom, area, or power consumption. Alternatively, an IP2 calibration scheme may be incorporated. All the existing circuits [1, 3, 4] introduce intentional asymmetry in the mixer to improve IP2. This approach suffers from a few drawbacks. First, depending on which source of mixer nonlinearity is dominant, a complete correction may not be achieved. Secondly, other mixer parameters may be adversely affected. In addition, they all propose a factory calibration. In this paper a different scheme based on an automatic dynamic current injection is introduced. The circuit allows the mixer to be designed and optimized independently, and has negligible impact on its noise figure, area, and power consumption.

Consider a direct down-converter whose 2nd-order nonlinearity is defined as follows:

$$y = a_1 x + a_2 x^2 \quad (1)$$

A blocker with an amplitude of A_B and frequency of $w_{LO} + w_B$ at the input results in the following components at the output:

$$y = \frac{a_2 A_B^{\ 2}}{2} + a_1 A_B Cos(\omega_B t) + \frac{a_2 A_B^{\ 2}}{2} Cos(2\omega_B t) \quad (2)$$

Although the last two terms are removed by the receiver channel-select filter at the down-converter output, the first term creates an undesirable dc offset, which corrupts the receiver SNR at baseband. The dc offset is *dynamic* in nature, as it depends on the blocker, and cannot be removed by a dc cancellation loop, which applies a constant dc voltage to the mixer output. Nonetheless, injecting a *dynamic* dc offset in the opposite direction, but proportional to the *blocker amplitude squared*, effectively eliminates the 2nd-order component and yields an infinite IIP2. Shown in Fig. 25.7.1, this new concept is implemented based on the square-law property of long channel FET's. The circuit input is connected to the outputs of the mixer. Thus, it takes the *down-converted blocker* whose amplitude is proportional to that of the RF blocker. An input with amplitude of A_{in} and frequency of w_{in} creates the following differential current at the output:

$$i_{od} = \pm\beta V_{in}^{\ 2} = \pm\frac{1}{2}\beta A_{in}^{\ 2} \pm \frac{1}{2}\beta A_{in}^{\ 2} Cos 2\omega_{in} t \quad (3)$$

Where $\beta = \mu C_{OX} W/L$ is process and transistor-size dependent. To create a balanced dc current at the outputs in the absence of blocker, a dummy current source (M_0) biased at the input dc level is employed. The ± term is determined by the sign bits, *P* and *N*. If both *P* and *N* are zero, no current is injected. Otherwise, one is zero, and the other one is high, and a signed current is injected to the mixer output. Figure 25.7.2 shows the complete schematic of the IP2 calibration circuit, which uses weighed replicas of the current source in Fig. 25.7.1. Five bits of coarse and fine control along with a sign bit are used. To set the bias of the current sources independently of the mixer dc level, an ac-coupling circuit whose corner frequency is chosen well below the blocker frequency is used. Switches controlled by the *Enable* signal are added to disconnect the input and leave the current sources connected to the dc bias voltage. This feature will be used in the automatic calibration process. The sizes of the current sources are set so that an IIP2 of as low as +35dBm in the mixer is corrected to at least +70dBm. Each of the I and Q mixers use a separate calibration circuit with independent sign and value controls.

Due to the random nature of the 2nd-order nonlinearity sources in the mixers, a calibration circuit is required. A *factory calibration* is not desirable, as it raises the testing time, and as a consequence, the cost. Moreover, it typically does not cover all the operating conditions, such as temperature and voltage variations. Figure 25.7.3 shows the proposed architecture for the *automatic calibration*, where the transmitter is used as a test blocker generator for the receiver. As the IP2 current sources are not frequency dependent, the exact frequency and amplitude of the test blocker is not important. Baseband ADC's used otherwise for demodulation are employed to measure the static and dynamic dc offset, and determine the correct amount of injection. Figure 25.7.4 shows the corresponding timing diagram. The calibration is performed during the transmit slot, where the receiver is turned on as well. The IP2 current source is set to a nominal value of C_0. Before the PA ramp starts, the residual dc offset of the receive chain is read by the ADC and stored (DC_0). Once the ramp is complete, the leakage from the PA output to the receiver input through the TR switch acts as a blocker and induces a dynamic dc offset. The receiver dc level is now measured with the calibration circuit first disabled (DC_1), and then enabled at the nominal setting (DC_2). The final value of the IP2 current setting is determined as follows:

$$C = C_0 \times \frac{DC_1 - DC_0}{DC_1 - DC_2} \quad (4)$$

To allow for a better correction, an *optional* LMS feedback algorithm in which the calibration is updated periodically is employed as well. It starts at an arbitrary initial value, and the current setting is slowly varied. Since the calibration needs to be updated only every few seconds for temperature and LMS adjustments, the power consumption overhead due to the receiver turning on during the transmit mode is negligible.

To validate this concept, the IP2 calibration circuit shown in Fig. 25.7.2 was fabricated and measured. To perform a full automatic calibration, baseband circuits comprising 8b ADC's, as well as the transmitter section as shown in Fig. 25.7.3 are included on the test chip. Figure 25.7.5 shows the simulated and measured dc induced-voltage at the output versus the blocker power at the input of the IP2 calibration circuit. The simulations and measurements agree well, and a slope of 40dB/dec is measured as expected. Figure 25.7.6 shows the mixer's measured IIP2 with and without calibration over 8 samples at 2GHz. An average IIP2 of 79.5dBm, and a minimum IIP2 of 73.1dBm are achieved. The average improvement is about 18dB. The circuit has little impact on the mixer IIP3, noise figure and other parameters.

The test chip was fabricated in TSMC 0.13μm CMOS technology. A micrograph of the IP2 calibration circuit is shown in Fig. 25.7.7. It occupies an area of 0.012mm^2, which is about 14% of the mixer area alone. Under nominal conditions, the circuit drains a current of 120μA from a 1.2V supply.

References:

[1] R. Magoon et al., "A Single-Chip Quad-Band (850/900/1800/1900 MHz) Direct-Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1710-1720, 2002.

[2] M. Brandolini et al., "A CMOS Direct Down-Converter with +78dBm Minimum IIP2 for 3G Cell-Phones," *ISSCC Dig. Tech. Papers*, pp. 320-321, Feb., 2005.

[3] K. Kivekas et al., "Calibration Techniques of Active BiCMOS Mixers," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 766-769, 2002.

[4] M. Hotti et al., "IIP2 Calibration Methods for Current Output Mixer In Direct-Conversion Receivers," *IEEE Int'l Symp. Circuits and Systems,* pp. 5059-5062, May, 2005.

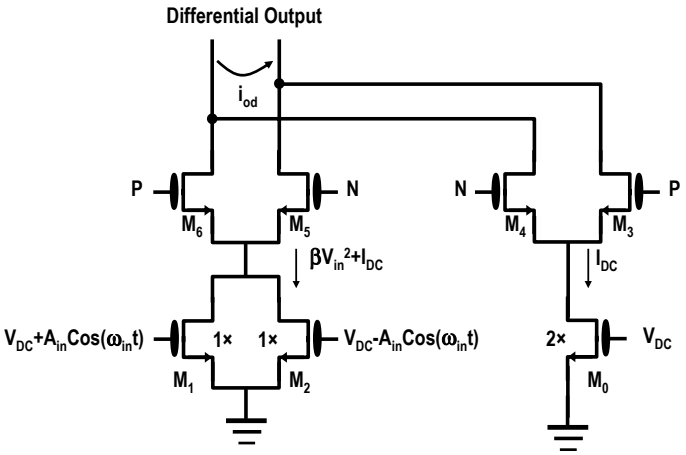

Figure 25.7.1: Circuit of dynamic dc offset injection.

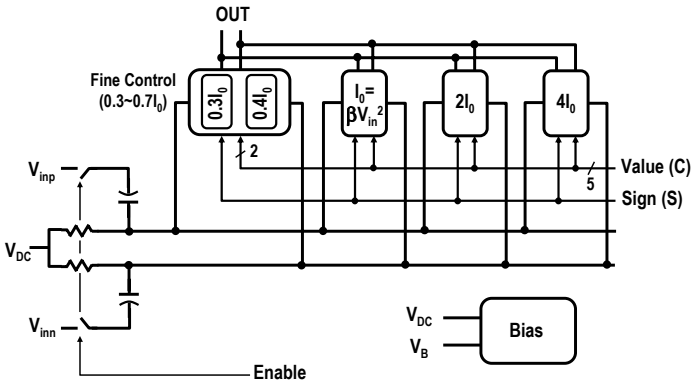

Figure 25.7.2: IP2 calibration circuit.

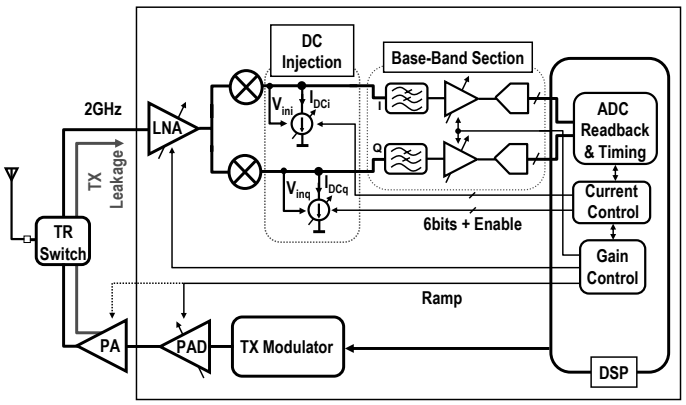

Figure 25.7.3: Automatic calibration architecture.

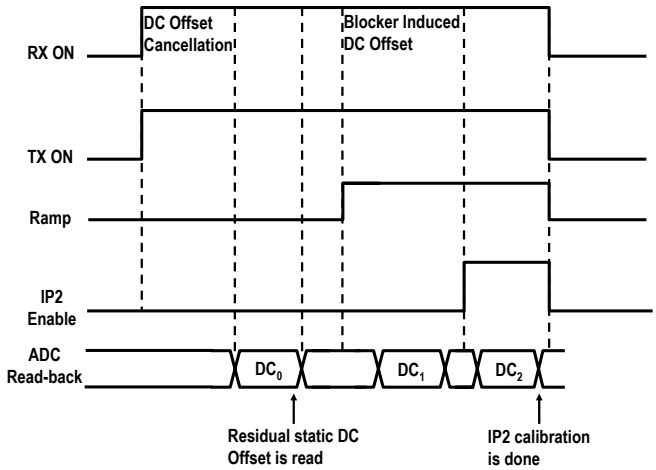

Figure 25.7.4: IP2 calibration timing diagram.

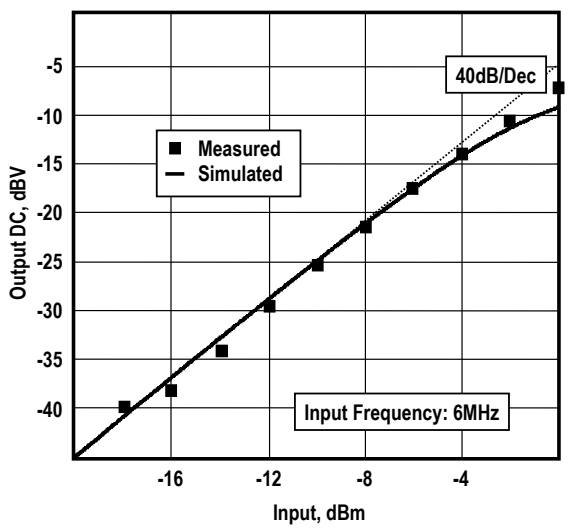

Figure 25.7.5: Calibration circuit output versus input power.

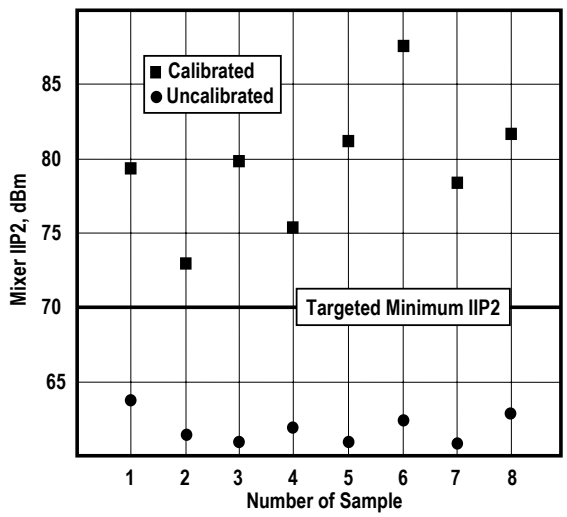

Figure 25.7.6: The mixer's measured IIP2 with and without calibration.

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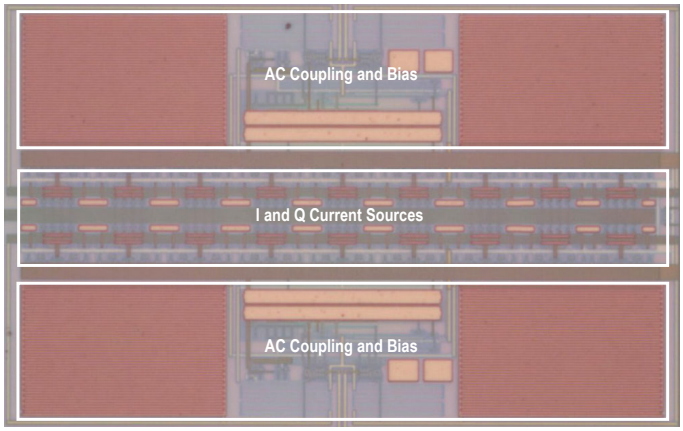

Figure 25.7.7: Die micrograph of I-Q IP2 calibration circuit.

